IN THE CLAIMS:

Please amend claims as follows:

6.(Amended) A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:

a mixer core having a doubly balanced mixer including a first differentially coupled [npn] transistor pair and a second differentially coupled [npn] transistor pair, the mixer core coupled to receive a LO drive signal, the LO drive signal having a plurality of harmonics;

a low noise RF input circuit coupled to the mixer core through a folded_cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the folded cascode circuit further isolates the RF input circuit from the LO drive signal and the plurality of harmonics.

7.(Amended) A mixer as in Claim 6 wherein the folded cascode circuit comprises:

a first cascode transistor having an emitter terminal coupled to a second terminal of a first capacitor and to a first terminal of a third inductor, a collector terminal coupled to the second differentially coupled [npn] transistor pair and a base terminal,

a second cascode transistor having a base terminal coupled to the base terminal of the first cascode transistor, an emitter terminal coupled to a first terminal of a second inductor and to an emitter terminal of a first [npn] transistor and a collector terminal coupled to the first differentially coupled [npn] transistor pair,

a second capacitor, having a first terminal coupled to the emitter terminal of the second cascode transistor and a second terminal coupled to a second terminal of the first capacitor, the base terminal of the first cascode transistor and to the base terminal of the second cascode transistor,

a third capacitor, having a first terminal coupled to the emitter terminal of the first cascode transistor and a second terminal coupled to the second terminal of the second capacitor,

a second biasing resistor having a first terminal coupled to the first terminal of the second capacitor and a second terminal coupled to a second bias voltage.

8.(Amended) A mixer as in Claim 7, wherein the low noise RF input circuit further includes a RF feedback circuit, the RF feedback circuit comprising:

a second [npn] transistor having a base terminal coupled to the supply potential, an emitter terminal coupled to the collector terminal of the first input [npn] transistor and a collector terminal coupled to the first terminal of the supply resistor and to the first terminal of the first capacitor,

a feedback resistor, having a first terminal coupled to the base terminal of the first input [npn] transistor and a second terminal,

a second capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

9.(Amended) A mixer as in Claim 7, wherein the mixer core further includes a tracking supply circuit, the tracking supply circuit comprising:

a first diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal,

a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal,

a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal,

a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential,

a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal,

a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal,

a second [npn] transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal,

a third [npn] transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second [npn] transistor and a collector terminal,

a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third [npn] transistor

a second current supply having a first terminal coupled to the emitter terminal of the second [npn] transistor and to the emitter terminal of the third [npn] transistor and a second terminal coupled to the ground potential,

a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third [npn] transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input,

a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential,

a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second [npn] transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input,

a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

10.(Amended) A mixer as in Claim 7, wherein the low noise RF input circuit further includes a tracking mixer bias current circuit coupled to the second bias input terminal, the tracking mixer bias current circuit comprising:

a third resistor having a first terminal coupled to the supply potential and a second terminal,

a first diode connected transistor having a anode terminal coupled to the second terminal of the third resistor and a cathode terminal,

a second [npn] transistor having a collector terminal coupled to the cathode terminal of the first diode connected transistor, an emitter terminal coupled to the ground potential and a base terminal,

a loop amplifier having a first terminal coupled to the emitter terminal of the first diode connected transistor and to the collector terminal of the second [npn] transistor, a second terminal coupled to the second bias voltage and a third terminal,

a fourth resistor having a first terminal coupled to the base terminal of the second [npn] transistor and a second terminal coupled to the second terminal of the loop amplifier and to the second bias voltage,

a bandgap voltage supply having a first terminal coupled to the ground potential and a second terminal coupled to the third terminal of the loop amplifier.

11.(Amended) A mixer circuit as in Claim 6, wherein the mixer core further includes a tracking supply circuit, the tracking supply circuit comprising:

a first diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal,

a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal,

a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal,

a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential,

a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal,

a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal,

a second [npn] transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal,

a third [npn] transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second [npn] transistor and a collector terminal,

a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third [npn] transistor

a second current supply having a first terminal coupled to the emitter terminal of the second [npn] transistor and to the emitter terminal of the third [npn] transistor and a second terminal coupled to the ground potential,

a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third [npn] transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input,

a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential,

a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second [npn] transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input,

a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

12.(Amended) A mixer circuit as in Claim 6, wherein the low noise RF input circuit further includes a RF feedback circuit coupled to the RF input circuit, the RF feedback circuit comprising:

a second [npn] transistor having a base terminal coupled to the supply potential, an emitter terminal coupled to the collector terminal of the first input [npn] transistor and a collector terminal coupled to the first terminal of the supply resistor and to the first terminal of the first capacitor,

a feedback resistor, having a first terminal coupled to the base terminal of the first input [npn] transistor and a second terminal,

a second capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

13.(Amended) A quadrature mixer circuit for generating a quadrature IF output responsive to an RF input and a quadrature pair of LO drive signals, comprising:

a mixer core having a first doubly balanced mixer including a first differentially coupled [npn] transistor pair and a second differentially coupled [npn] transistor pair and a second doubly balanced mixer including a third differentially coupled [npn] transistor pair and a fourth differentially coupled [npn] transistor pair;

an RF input circuit coupled to the mixer core, the RF input circuit comprising:

an input inductor having a first terminal coupled to receive an RF input signal and a second terminal;

a biasing resistor having a first terminal coupled to the second terminal of the input inductor and a second terminal coupled to a first bias voltage;

a first input [npn] transistor having a base terminal coupled to the second terminal of the input inductor, an emitter terminal, and a collector terminal;

a second inductor having a first terminal coupled to the emitter of the first [npn] transistor and to the first differentially coupled [npn] transistor pair and to the third differentially coupled [npn] transistor pair, the second inductor also having a second terminal coupled to a ground potential;

a supply resistor having a first terminal coupled to the collector of the first transistor and a second terminal coupled to a supply potential;

a first capacitor having a first terminal also coupled to the collector of the first transistor and a second terminal coupled to the second differentially coupled [npn] transistor pair and to the fourth differentially coupled [npn] transistor pair; and

a third inductor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the ground potential.

14.(Amended) A quadrature mixer circuit for generating a quadrature IF output responsive to an RF input and a quadrature pair of LO drive signals, comprising:

a mixer core having a first doubly balanced mixer including a first differentially coupled [npn] transistor pair and a second differentially coupled [npn] transistor pair and having a second doubly balanced mixer including a third differentially coupled [npn] transistor pair and a fourth differentially coupled [npn] transistor pair; the mixer core coupled to receive a quadrature LO drive signal, the quadrature LO drive signal having a plurality of harmonics;

a low noise RF input circuit coupled to the mixer core through a folded cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the folded cascode circuit further isolates the RF input circuit from the quadrature LO drive signal and the plurality of harmonics,

a first cascode capacitor, a first terminal of the first cascode capacitor coupled to the emitter terminal of a first cascode transistor and a second node of the first cascode capacitor coupled to the base terminals of the first cascode transistor and a second cascode transistor,

a second cascode capacitor, a first terminal of the second cascode capacitor coupled to the base terminals of the first cascode transistor and the second cascode transistor and the second node of the second cascode capacitor coupled to the emitter terminal of the second cascode transistor.

15.(Amended) A quadrature mixer as in Claim 14 wherein the cascode circuit comprises:

a first cascode transistor having an emitter terminal coupled to the second terminal of the first capacitor and to the first terminal of the third inductor, a collector terminal coupled to the second differentially coupled [npn] transistor pair and a base terminal,

a second cascode transistor having a base terminal coupled to the base terminal of the first cascode transistor, an emitter terminal coupled to the first terminal of the second inductor and to the emitter terminal of the first [npn] transistor and a collector terminal coupled to the first differentially coupled [npn] transistor pair,

a second capacitor, having a first terminal coupled to the collector terminal of the first cascode transistor and a second terminal coupled to the base terminal of the first cascode transistor and to the base terminal of the second cascode transistor,

a third capacitor, having a first terminal coupled to the emitter terminal of the second cascode transistor and a second terminal coupled to the second terminal of the second capacitor and to the base terminal of the first cascode transistor and to the base terminal of the first cascode transistor,

a second biasing resistor having a first terminal coupled to the second terminal of the second capacitor and the first terminal of the third capacitor and a second terminal coupled to a second bias voltage,

a third biasing resistor having a first terminal coupled to the second bias voltage and to the second terminal of the second biasing resistor and having a second terminal,

a third cascode transistor having a collector terminal coupled to the fourth differentially coupled [npn] transistor pair, an emitter terminal coupled to the second terminal of the third inductor and to the emitter terminal of the first cascode transistor, and a base terminal,

a fourth cascode transistor having a base terminal coupled to the base terminal of the third cascode transistor, a collector terminal coupled the third differentially coupled [npn] transistor pair and an emitter terminal coupled to the emitter terminal of the second cascode transistor and to the second terminal of the second inductor,

a fourth capacitor having a first terminal coupled to the emitter terminal of the third cascode transistor and a second terminal coupled to the base terminal of the third and fourth cascode transistors,

a fifth capacitor having a first terminal coupled to the second terminal of the fourth capacitor and to the base terminals of the third and fourth cascode transistors and a second terminal coupled to the emitter terminal of the fourth cascode transistor.

16.(Amended) A quadrature mixer as in Claim 15 wherein the low noise RF input circuit further includes a RF feedback circuit, the RF feedback circuit comprising:

a second [npn] transistor having a base terminal coupled to the supply potential, an emitter terminal coupled to the collector terminal of the first input [npn] transistor and a collector terminal coupled to the first terminal of the supply resistor and to the first terminal of the first capacitor,

a feedback resistor, having a first terminal coupled to the base terminal of the first input [npn] transistor and a second terminal,

a sixth capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

18.(Amended) A mixer circuit as in Claim 17, wherein the first tracking supply comprises:

a. a first diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal;
b. a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal,
c. a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal;
d. a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential;
e. a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal;
f. a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal;
g. a second [npn] transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal;
h. a third [npn] transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second [npn] transistor and a collector terminal;

i. a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third [npn] transistor;

j. a second current supply having a first terminal coupled to the emitter terminal of the second [npn] transistor and to the emitter terminal of the third [npn] transistor and a second terminal coupled to the ground potential;

k. a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third [npn] transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input;

l. a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential;

m. a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second [npn] transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input; and

n. a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential;

and wherein the second tracking supply circuit portion comprises:

o. a third diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal;

p. a fourth diode-connected transistor having a cathode terminal coupled to the anode terminal of the third diode connected transistor and an anode terminal;

q. a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal;

r. a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential;

s. a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal;

t. a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal;

u. a second [npn] transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal;

v. a third [npn] transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second [npn] transistor and a collector terminal;

w. a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third [npn] transistor;

x. a second current supply having a first terminal coupled to the emitter terminal of the second [npn] transistor and to the emitter terminal of the third [npn] transistor and a second terminal coupled to the ground potential;

y. a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third [npn] transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input;

z. a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential;

aa. a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second [npn] transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input;

ab. a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

19.(Amended) A quadrature mixer as in Claim 15, wherein the low noise RF input circuit further includes a tracking mixer bias current circuit, the tracking bias current circuit comprising:

a first resistor having a first terminal coupled to the supply potential and a second terminal,

a first diode connected transistor having a anode terminal coupled to the second terminal of the third resistor and a cathode terminal,

a second [npn] transistor having a collector terminal coupled to the cathode terminal of the first diode connected transistor, an emitter terminal coupled to the ground potential and a base terminal,

a loop amplifier having a first terminal coupled to the emitter terminal of the first diode connected transistor and to the collector terminal of the second [npn] transistor, a second terminal coupled to the second bias voltage and a third terminal,

a second resistor having a first terminal coupled to the base terminal of the second [npn] transistor and a second terminal coupled to the second terminal of the loop amplifier and to the second bias voltage,

a bandgap voltage supply having a first terminal coupled to the ground potential and a second terminal coupled to the third terminal of the loop amplifier.

20.(Amended) A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:

a mixer core having a doubly balanced mixer including a first differentially coupled [npn] transistor pair and a second differentially coupled [npn] transistor pair;

a single ended RF input circuit coupled to receive an RF signal, the RF circuit coupled to the mixer core, the RF circuit including means for providing an input impedance, means for splitting a phase of the RF signal, and means for decoupling noise from the RF signal to the mixer core.

21.(Amended) A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:

a mixer core having a doubly balanced mixer including a first differentially coupled [npn] transistor pair and a second differentially coupled [npn] transistor pair, the mixer core coupled to receive a LO drive signal, the LO drive signal having a plurality of harmonics;

a low noise single ended RF input circuit coupled to the mixer core through a cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the cascode circuit further isolates the RF input circuit from the LO drive signal and the plurality of

harmonics the RF circuit including means for providing an input impedance and means for splitting a phase of the RF signal.

22. (New) The mixer circuit according to Claim 6 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all npn transistors.

23.(New) The mixer circuit according to Claim 6 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all pnp transistors.

24.(New) The mixer circuit according to Claim 6 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MOSFET transistors.

25.(New) The mixer circuit according to Claim 6 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MESFET transistors.

26. (New) The mixer circuit according to Claim 13 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all npn transistors.

27.(New) The mixer circuit according to Claim 13 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all pnp transistors.

28.(New) The mixer circuit according to Claim 13 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all MOSFET transistors.

29.(New) The mixer circuit according to Claim 13 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all MESFET transistors.

31. (New) The mixer circuit according to Claim 14 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all npn transistors.

32.(New) The mixer circuit according to Claim 14 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all pnp transistors.

33.(New) The mixer circuit according to Claim 14 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all MOSFET transistors.

34.(New) The mixer circuit according to Claim 14 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair, the third differentially coupled transistor pair, the fourth differentially coupled transistor pair and the first input transistor are all MESFET transistors.

35. (New) The mixer circuit according to Claim 20 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all npn transistors.

36.(New) The mixer circuit according to Claim 20 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all pnp transistors.

37.(New) The mixer circuit according to Claim 20 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MOSFET transistors.

38.(New) The mixer circuit according to Claim 20 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MESFET transistors.

39. (New) The mixer circuit according to Claim 21 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all npn transistors.

40.(New) The mixer circuit according to Claim 21 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all pnp transistors.

41.(New) The mixer circuit according to Claim 21 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MOSFET transistors.

42.(New) The mixer circuit according to Claim 21 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MESFET transistors.

REMARKS

The Applicants respectfully request further examination and reconsideration in view of the above preliminary amendment. By this preliminary amendment applicants have amended claims 6-16 and 18-21, and added new claims 22-42. Accordingly, after the above preliminary amendment claims 1-42 are now pending.

Applicants respectfully submit that the claims, as amended, are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: 8-29-02

By: _____
Thomas B. Haverstock
Reg. No.: 32,571
Attorneys for Applicants